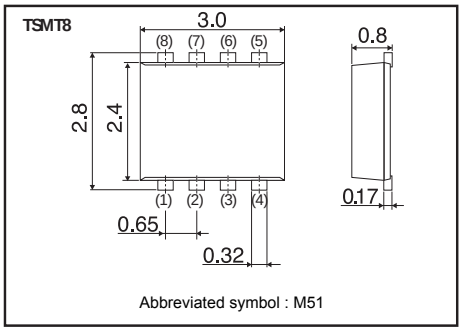
4V Drive Nch + Pch MOSFET

QS8M51

● Structure
Silicon N-channel MOSFET/
Silicon P-channel MOSFET

● Features
1) Low on-resistance.
2) Low voltage drive (4V drive).
3) Small surface mount package (TSMT8).

● Dimensions (Unit : mm)

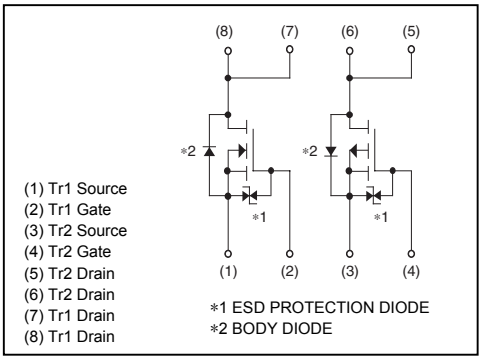


● Application
Switching

● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8M51		○

● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	100	−100	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	Continuous	I_D	±2	±1.5	A
	Pulsed	I_{DP} *1	±6	±6	A
Source current (Body Diode)	Continuous	I_s	1.0	−1.0	A
	Pulsed	I_{sp} *1	6	−6	A
Power dissipation		P_D *2	1.5		W / TOTAL
			1.25		W / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

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● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=100V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	1	-	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	240	325	mΩ	I_D=2A, V_{GS}=10V
		-	250	340		I_D=2A, V_{GS}=4.5V
			260	355		I_D=2A, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$*	1.9	-	-	S	V_{DS}=10V, I_D=2A
Input capacitance	C_{iss}	-	290	-	pF	V_{DS}=25V
Output capacitance	C_{oss}	-	30	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	20	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$ *	-	10	-	ns	V_{DD}≒ 50V, I_D=1A
Rise time	t_r *	-	10	-	ns	V_{GS}=10V
Turn-off delay time	$t_{d(off)}$ *	-	30	-	ns	R_L=50Ω, R_G=10Ω
Fall time	t_f *	-	15	-	ns	
Total gate charge	Q_g *	-	4.7	-	nC	V_{DD}≒ 50V, I_D=2A
Gate-source charge	Q_{gs} *	-	1.2	-	nC	V_{GS}=5V
Gate-drain charge	Q_{gd} *	-	1.8	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	1.2	V	I_s=2A, V_{GS}=0V

*Pulsed

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● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−100	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	−1	μA	V_{DS}=−100V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	−1	-	−2.5	V	V_{DS}=−10V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS(on)}$*	-	350	470	mΩ	I_D=−1.5A, V_{GS}=−10V
		-	380	510		I_D=−0.75A, V_{GS}=−4.5V
			400	540		I_D=−0.75A, V_{GS}=−4V
Forward transfer admittance	$\|Y_{fs}\|$*	1.5	-	-	S	V_{DS}=−10V, I_D=−1.5A
Input capacitance	C_{iss}	-	950	-	pF	V_{DS}=−25V
Output capacitance	C_{oss}	-	45	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	20	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	10	-	ns	V_{DD}≒ −50V, I_D=−0.75A
Rise time	t_r *	-	15	-	ns	V_{GS}=−10V
Turn-off delay time	$t_{d(off)}$*	-	60	-	ns	R_L=66Ω, R_G=10Ω
Fall time	t_f *	-	10	-	ns	
Total gate charge	Q_g *	-	17	-	nC	V_{DD}≒ −50V, I_D=−1.5A
Gate-source charge	Q_{gs} *	-	4.5	-	nC	V_{GS}=−5V
Gate-drain charge	Q_{gd} *	-	5	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−0.75A, V_{GS}=0V

*Pulsed

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●Electrical characteristic curves (Ta=25°C)

〈Tr.1(Nch)〉

Fig.1 Typical Output Characteristics (Ⅰ)

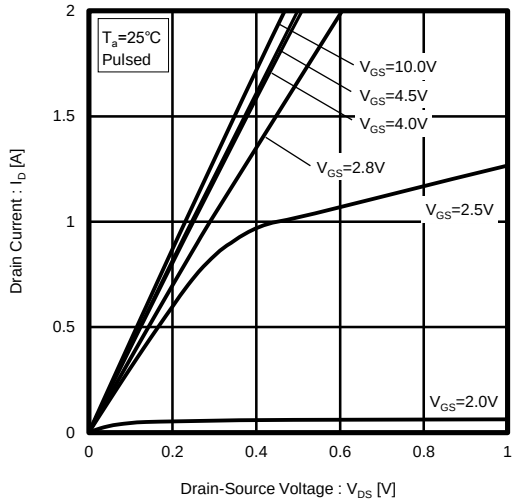

Fig.2 Typical Output Characteristics (Ⅱ)

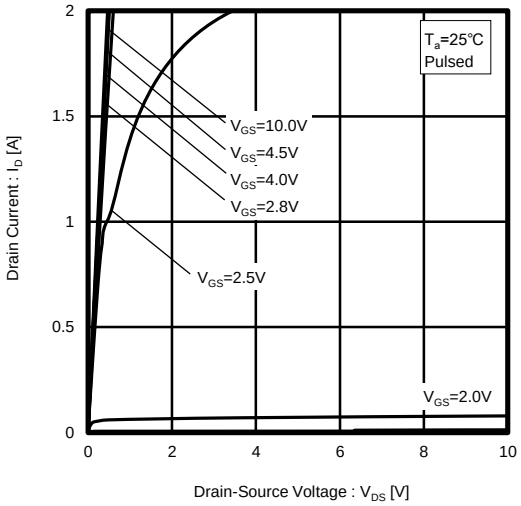

Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

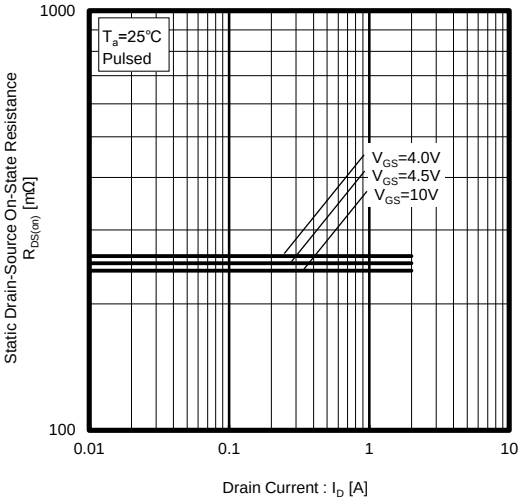

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

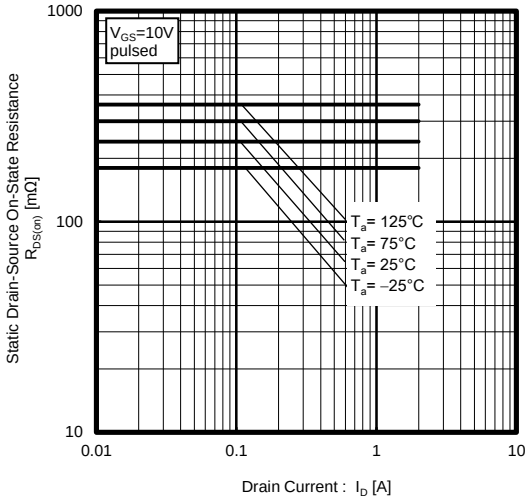

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

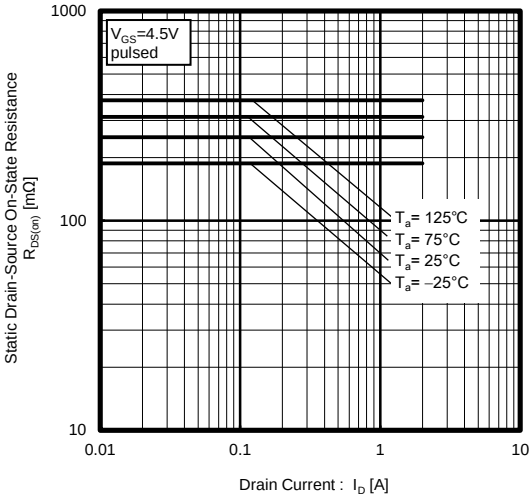

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

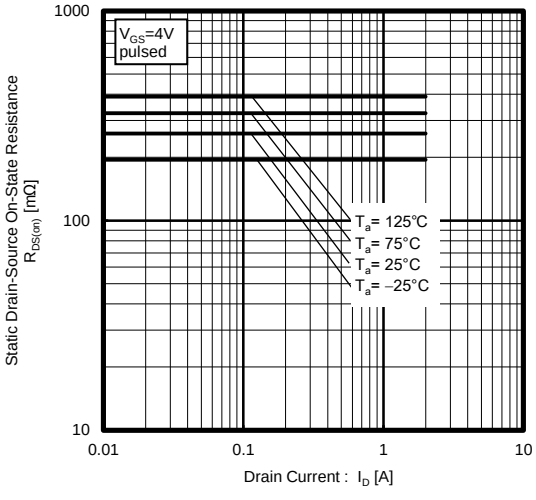

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Fig.7 Forward Transfer Admittance vs. Drain Current

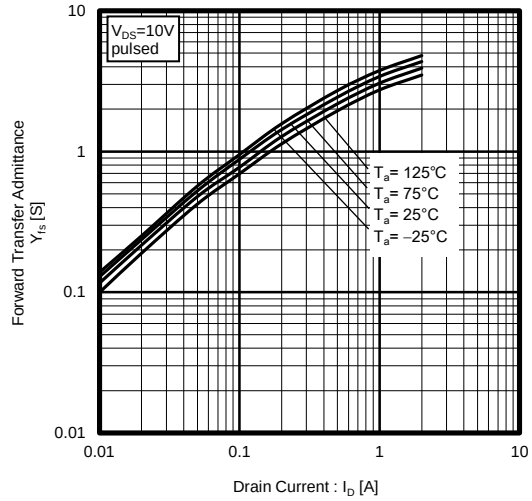

Fig.8 Typical Transfer Characteristics

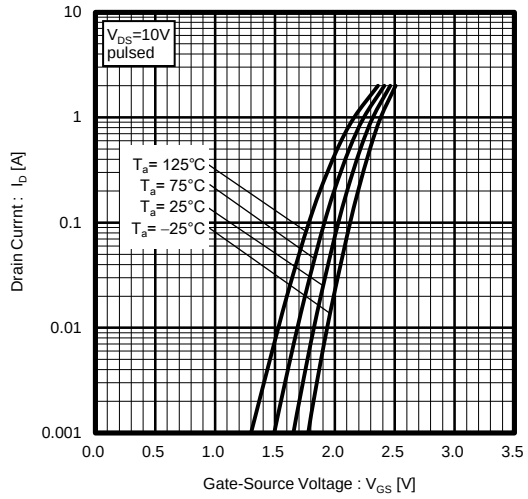

Fig.9 Source Current vs. Source-Drain Voltage

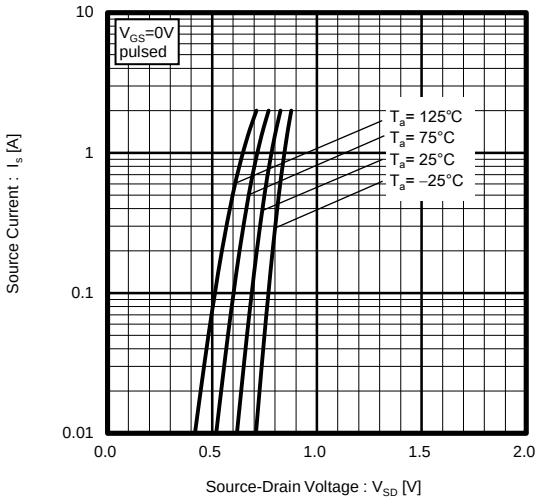

Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

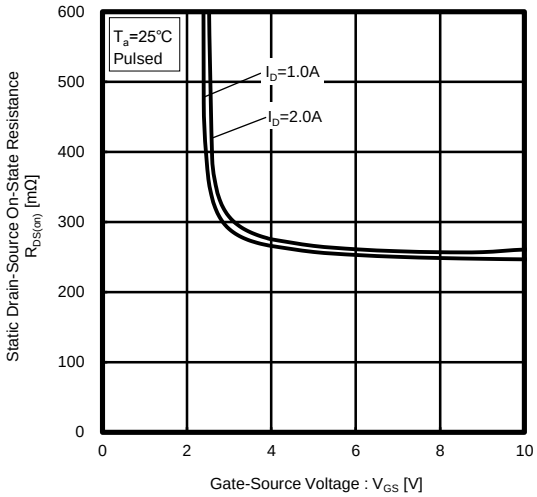

Fig.11 Switching Characteristics

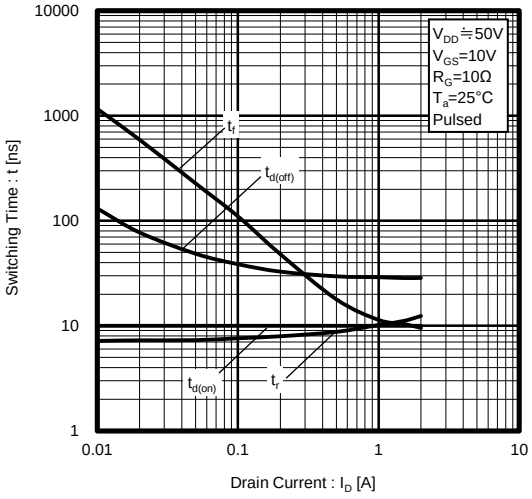

Fig.12 Dynamic Input Characteristics

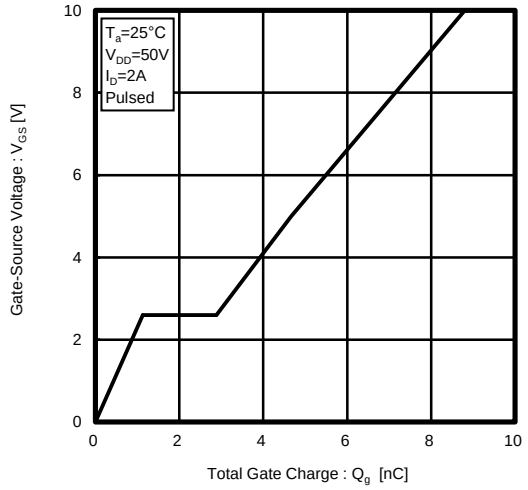

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Fig.13 Typical Capacitance vs. Drain-Source Voltage

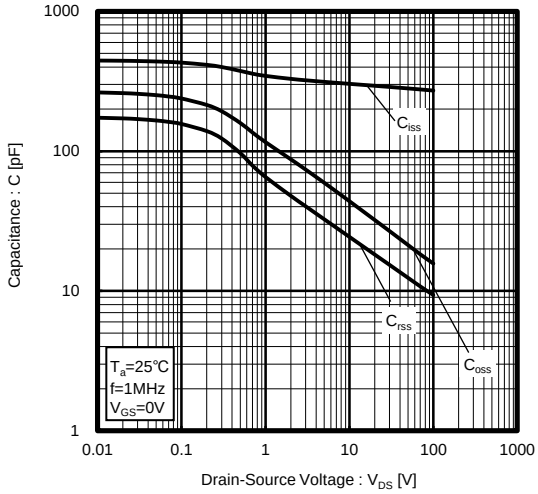


Fig.14 Normalized Transient Thermal Resistance v.s. Pulse Width

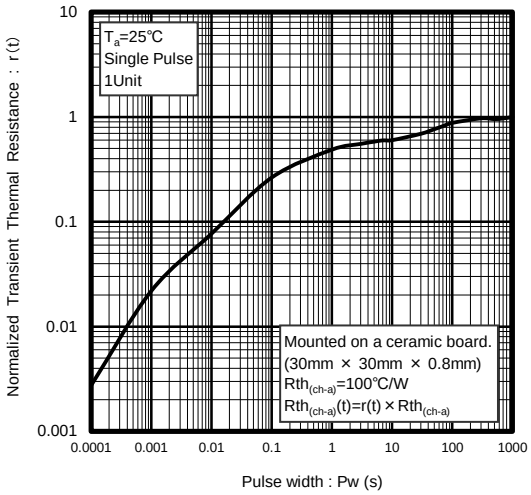
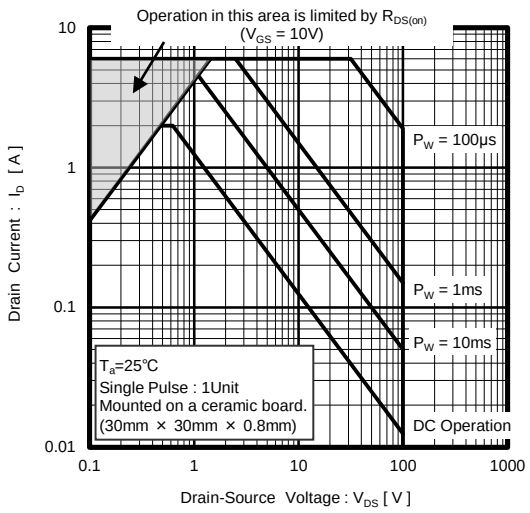


Fig.15 Maximum Safe Operating Area



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〈Tr.2(Pch)〉

Fig.1 Typical Output Characteristics (Ⅰ)

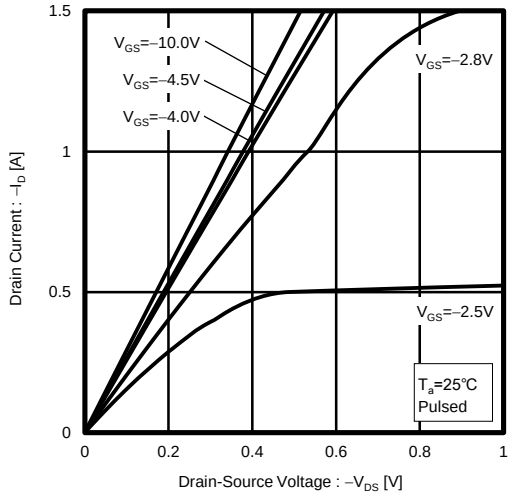

Fig.2 Typical Output Characteristics (Ⅱ)

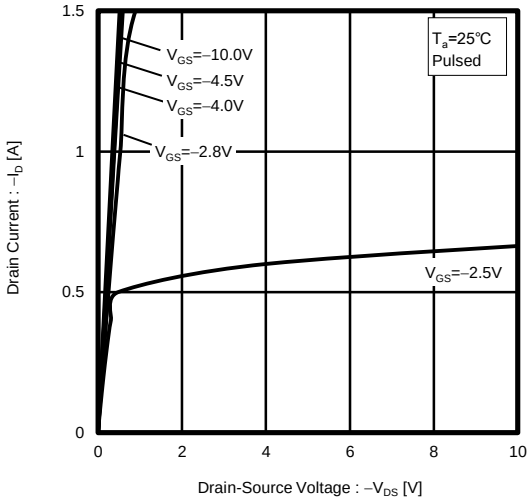

Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

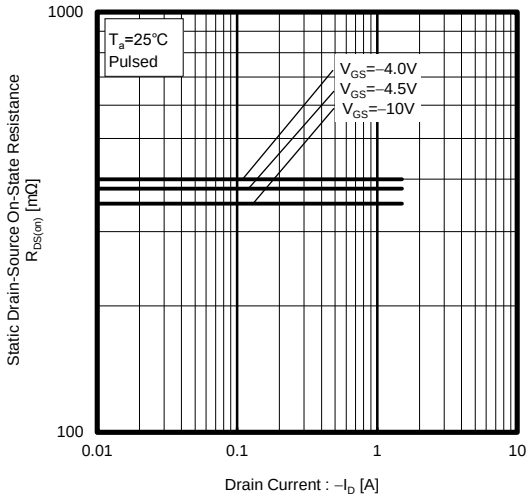

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

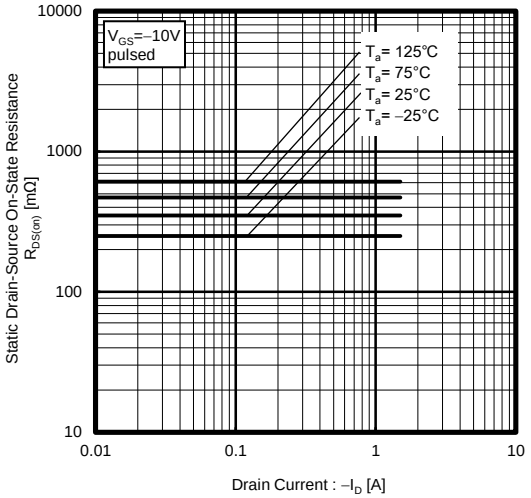

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

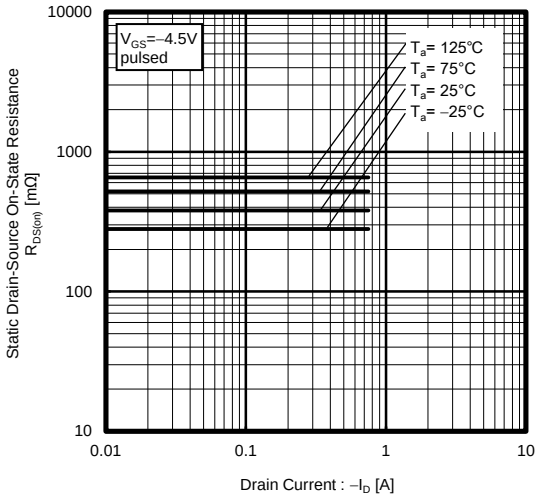

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

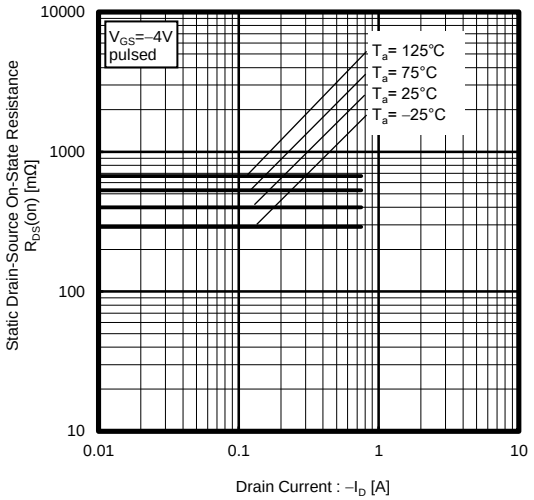

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Fig.7 Forward Transfer Admittance vs. Drain Current

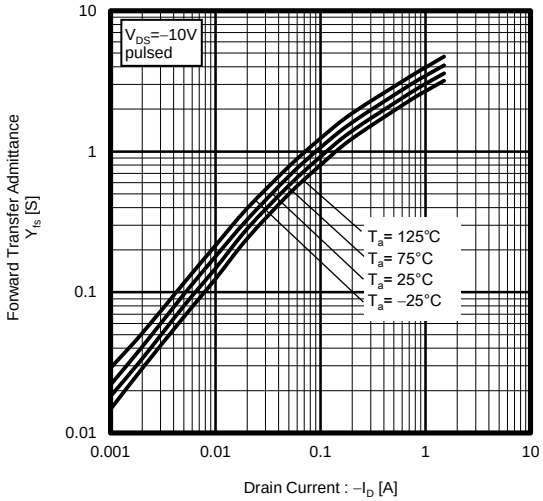

Fig.8 Typical Transfer Characteristics

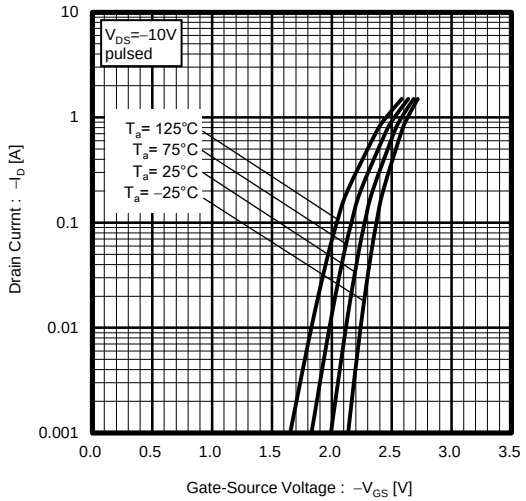

Fig.9 Source Current vs. Source-Drain Voltage

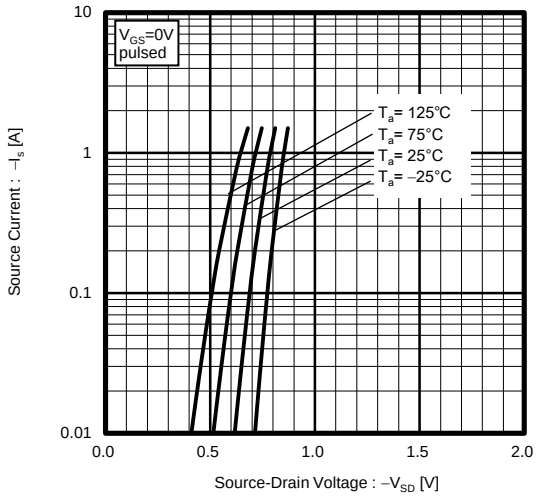

Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

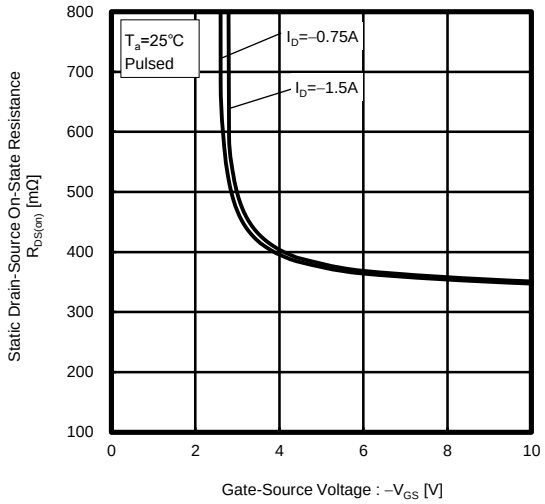

Fig.11 Switching Characteristics

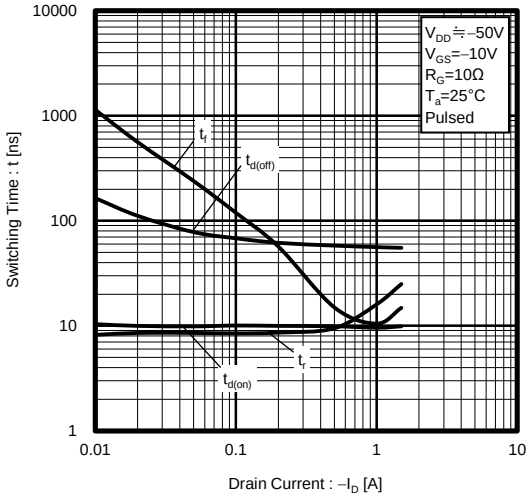

Fig.12 Dynamic Input Characteristics

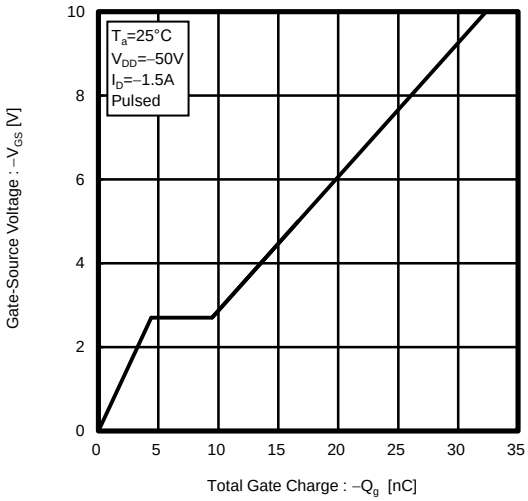

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Fig.13 Typical Capacitance vs. Drain-Source Voltage

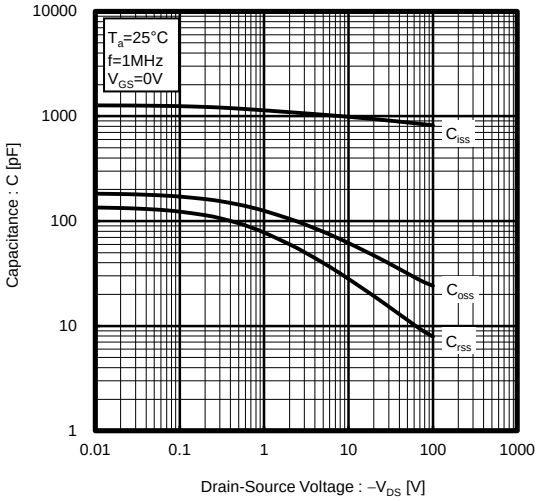


Fig.14 Normalized Transient Thermal Resistance v.s. Pulse Width

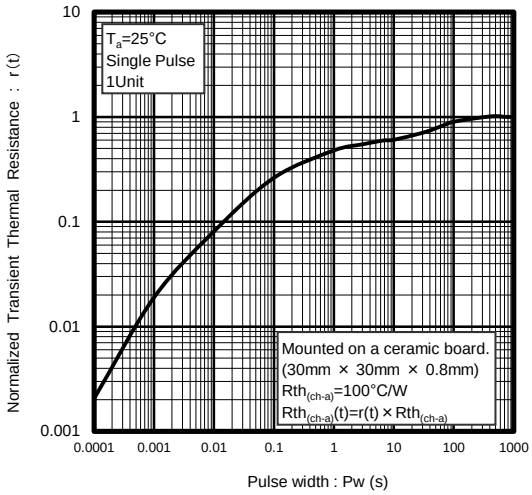
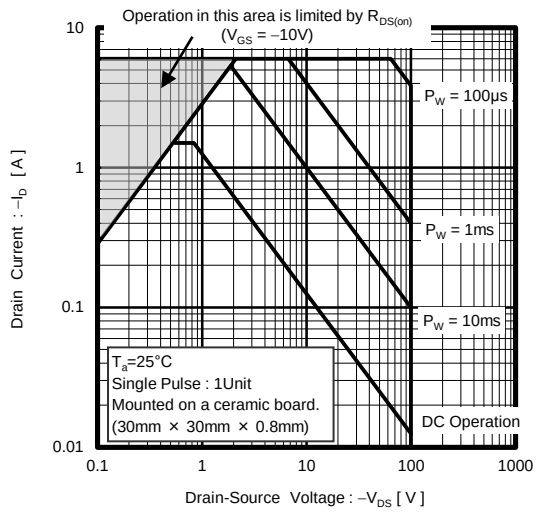


Fig.15 Maximum Safe Operating Area



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● **Measurement circuits**

<Tr1(Nch)>

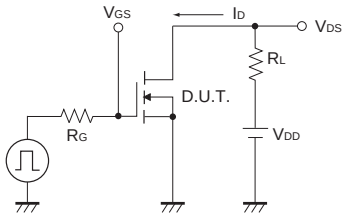

Fig.1-1 Switching Time Measurement Circuit

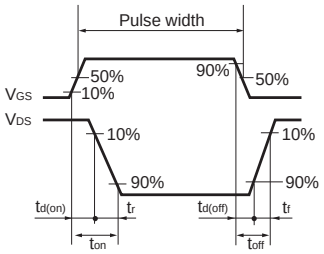

Fig.1-2 Switching Waveforms

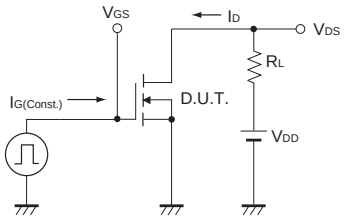

Fig.2-1 Gate Charge Measurement Circuit

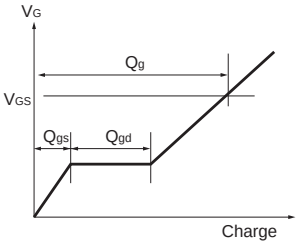

Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

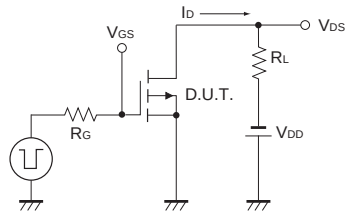

Fig.1-1 Switching Time Measurement Circuit

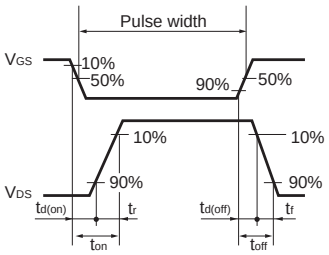

Fig.1-2 Switching Waveforms

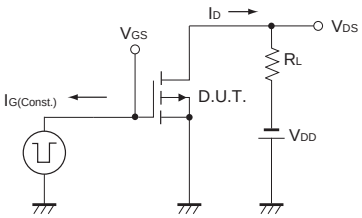

Fig.2-1 Gate Charge Measurement Circuit

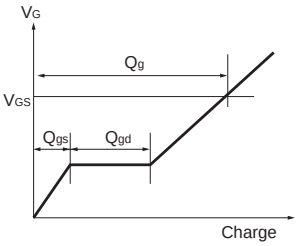

Fig.2-2 Gate Charge Waveform

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